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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,617	05/31/2000	Rama R. Goruganthu	AMDA.441PA	2990

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EXAMINER	
SOUW, BERNARD E	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,617	GORUGANTHU ET AL.	
	Examiner	Art Unit	
	Bernard E Souw	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-19 and 22-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-19 and 22-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. The Amendment filed on 08/23/2004 in response to the office action mailed 05/24/2004 has been entered. The present Office Action is made with all the suggested amendments being fully considered.

Claims 2, 3, 20 and 21 have been cancelled.

The independent claims 1, 16, and 17 have been amended.

Pending in this office action are claims 1, 4-19 and 22-29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-12, 16-19, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (USPAT # 6,137,295) in view of Talbot et al. (USPAT #6,091,249) or Steffan et al. (USPAT #6,200,823 B1).

► Regarding claims 1, 16 and 17, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1 (referring to claims 1, 16 and 20), the method comprising:

- removing substrate 1a shown in Fig.1 from the back side of the semiconductor die and exposing a region 1c of the insulator of the SOI structure, as recited in Col.5/ll.8-13; and
- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in Col.5/ll.19-32, and therefrom, analyzing the die, as recited in Col.5/ll.52-60;
- wherein the step of inducing a detectable response includes the use of an electron beam (EB) 15, as shown by Yoshida in Fig.2 and recited in Col.1/ll.10-13 + 25-33 and in Col.5/ll.19-32 + 53-55; wherein it is to be particularly noted that the term ***EB*** is *specifically defined* as being an "electron beam" by Yoshida in Col.1/line 11, which is to be distinguished from the term "*EB* ***tester***" that includes a (secondary electron) detector 10, as shown in Fig.13 and recited in Col.1/ll.62-67 and Col.2/ll.1-14
- wherein the step of detecting secondary electrons generated by the electron beam and the circuitry for analyzing the semiconductor die is expressly recited by Yoshida in Col.1/ll.25-33 and in Col.5/ll.19-32 + 53-55.

However, Yoshida's device and/or method does not recite to specifically use a scanning electron microscope to analyze the die, although Yoshida is using an electron beam EB 15, as expressly defined in Col.1/line 11, which is to be distinguished from the term "*EB* ***tester***" that includes a (secondary electron) detector 10, as shown in Fig.13 and recited in Col.1/ll.62-67 and Col.2/ll.1-14. The specific use of a scanning electron microscope (SEM) to generate the electron beam EB (Yoshida's EB 10) and to analyze the die based on the information carried by the secondary electrons (detected by

Yoshida's electron detector 10) is rendered obvious by Talbot et al. in Col.3/ll.13-16 & Col.6/ll.59-60 or Steffan et al. in Col.1/ll.64-67, wherein Talbot's and/or Steffan's method using SEM, as recited, replace(s) Yoshida's method of using an EB-***tester***.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the electron beam part of an SEM to replace Yoshida's EB, and further, to detect the secondary electrons as taught by Talbot et al. and/or Steffan et al., as recited above, in place of using Yoshida's EB ***tester***, since an SEM is a versatile apparatus that can be used for a variety of other purposes with high accuracies and a lot of device sophistication such as automated & computerized alignment, optics adjustment and device performance optimization, such as sample imaging and image processing, as compared to the EB ***tester*** used by Yoshida, which is usually much simpler and very specific in design and structure, while being also limited in the variety of tasks it is capable to execute.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to design Talbot's and/or Steffan's SEM apparatus, especially owing to its versatility, as recited above, to include all the functions of Yoshida's EB tester, since such a design is very well within skill in the art.

► Regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by Yoshida's device 1X in Fig.3, which consists of a plurality of circuit portions (1s & 1f) of Fig.1, which represents voltage variations across the plurality of circuit portions, resulting in a waveform shown in Fig.3, as recited in Col.5/ll.53-67.

► Regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited by Yoshida in Col.5/ll.57-67 and Col.6/ll.1-6, as shown in Fig.3 and Fig.4.

► Regarding claim 6, the step of using a pulsed EB is disclosed by Yoshida in Col.6/ll.1-6.

► Regarding claim 7, the step of using a coupling power supply and inputting electrical signals to the die to generate a response is inherent in Yoshida's, as implicated by the testing set 11 shown in Fig.2, recited in Col.5/ll.53-60, which inherently and conventionally includes a power supply.

As previously indicated, Yoshida's EB-tester, which includes Yoshida's DUT, is here to be replaced by Talbot's and/or Steffan's testing device that is capable of implementing the same tasks as the original Yoshida's DUT. For simplicity, in this office action these specific tasks and the specific units designed by one of ordinary skill in the art to accomplish those tasks will be hereinafter addressed by their equivalent DUT's tasks and units.

► Regarding claim 8, Yoshida's detectable response is obtained from source/drain region 1e (S/D = diffusion region) shown in Fig.1, as disclosed in Col.5/ll.1-5.

► Regarding claim 9, the step of using the BOX layer 1c in Fig.1 as a dielectric in inducing a detectable response, is disclosed by Yoshida in Col.5/ll.55-63, i.e., the potential waveform and potential contrast image shown in Fig.3.

► Regarding claim 10, the step of removing a portion of the substrate 1a to expose a portion of the BOX 1c is shown by Yoshida in Fig.1 and recited in Col.5/ll.8-32.

► Regarding claim 11, Yoshida's method is a post-manufacturing analysis because the device is analyzed after its manufacture is completed, as recited in Col.6/ll.14-19.

► Regarding claim 12, the electrical stimulus applied to the circuitry in the die is provided by *(Talbot's and/or Steffan's equivalent of)* the DUT board 12 shown in Fig.2, recited in Col.5/ll.43-48.

► Claims 16 and 17 are apparatus (system) claims reciting limitations that are already rejected along with claim 1. The additional recitation of a detector in claim 17 is shown by Yoshida as numeral 14 in Fig.2, as is inherent in Col.5/ll.56-60.

► Regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the BOX layer as an etching stop to control the substrate removal process, as recited in Col.5/ll.33-41, specifically in Col.5/line 39.

► Regarding claim 23, the step of using a tester adapter to introduce electrical stimulus to the die is disclosed in *(Talbot's and/or Steffan's equivalent of)* testing set 11 shown in Fig.2, as recited Col.5/ll.53-60.

3. Claims 13 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. or Steffan et al., and further in view of Zingher (USPAT #4,443,278), Gauthier et al. (USPAT # 4,172,228), and Nakasuji (USPAT #6,465,783),.

Yoshida as modified by Talbot et al. or Steffan et al. shows all the limitations of claims 13 and 24, as previously applied to the parent claim 12, except the recitation of inputting signals (to stimulate a response) until a failure is induced in the die.

Whether or not to use *Talbot's or Steffan's modification of* Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die, is a mere matter of deliberate choice, and hence, the step is unpatentable for only involving routine skill in the art, as already brought up in all previous Office Actions. Such a step is also conventional, as recited by Zingher in Col.4/ll.57-60, and further, by Gauthier et al. in Col.1/18-27. Furthermore, such a step is usually inherent in the last stages of semiconductor device manufacturing, as recited by Nakasuji in Col.18/ll.20-22 in reference to Step 17 of Fig.10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die, as taught by Gauthier et al. and Zingher, in order to implement a durability testing in semiconductor device manufacturing process, as taught by Nakasuji, since such testing is important for quality control.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. or Steffan et al., and further in view of Ishihara et al. (USPAT #6,185,324).

Yoshida as modified by Talbot et al. or Steffan et al. shows all the limitations of claim 14, as previously applied to the parent claim 12, except the specific recitation of

inputting signals in a continuous loop. In most automated processes, inputting signals in a continuous loop is part of the automation process, which is not patentable, because it merely replaces a conventional method that has been normally implemented manually. *In re Venner*, 120 USPQ 192.

Note that "manually" in this regard means that said step(s) may still be part of an automated or computerized process, but a person is involved for monitoring the process and making quick decision and countermeasure where necessary. By inputting the signals in a continuous loop in a fully automated process, monitoring, decision-making and implementing countermeasure are performed automatically performed by inputting and processing the signals in a continuous loop. Such a practice is well known in the art of semiconductor device manufacturing, as recited by Ishihara et al. in the Abstract and in reference of Fig.1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the data regarding a semiconductor circuit under test into a fully automated production or testing process by putting the data signals in a continuous loop, in order to provide a semiconductor failure analysis in which the cause of a failure is examined easily, accurately and speedily, as taught by Ishihara et al. in Col.2/ll.30-35.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. or Steffan et al., and further in view of Lo et al. (USPAT 6,344,750, hereinafter denoted as Lo'750) and Cole, Jr. (USPAT #5,523,694).

Yoshida as modified by Talbot et al. or Steffan et al. shows all the limitations of claim 5, as previously applied to the parent claim 1, except the recitation of using a non-defective die as a reference. More specifically, Talbot et al. disclose a method for analyzing a semiconductor die using an electron beam from a SEM 20 shown in Fig.1, as recited in Col.5/ll.33-57. Talbot's apparatus and method make use of a defect-free device as reference, as recited in Col.6/ll.65-67.

It would have been obvious to adopt Talbot's use of a non-defective die as a reference in Yoshida's method, since from a single image of a device alone *in the absence of other information*, it is difficult to determine whether or not the device under testing (DUT) contains an error, as implicated by Talbot et al. in Col.6/ll.63-65.

One would have been motivated to compare the equivalent EB image of a DUT with a known, non-defective device, as used by Talbot et al., since a defective die would be much more easily and much more quickly recognized by an operator, especially when the image of the non-defective die is subtracted from the currently measured image of a DUT (die under testing), thus highlighting the defect, as suggested by Steffan et al. in Col.3/ll.8-13.

The specific wording "*comparing*" the analysis of the dies is expressly recited by Lo'750 in the Abstract/ll.1-5, whereas Cole, Jr. performs various secondary electron image processing as disclosed in Applicant's specification, including adding, subtracting, enhancing, digitizing, storing and many other steps conventional to image processing, as recited in Col.9/ll.37-49.

It would have been obvious to adopt Lo'750's method of comparing the analysis of the dies while performing Cole's various image processing steps, in order to expedite and simplify the electron beam inspection process of Yoshida as modified by Talbot et al. and/or Steffan et al.

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. or Steffan et al., and further in view of Kim et al. (USPAT #2002/0043628A1) and Yamazaki et al. (USPAT #6,038,018).

Yoshida as modified by Talbot et al. or Steffan et al. shows all the limitations of claim 22, as previously applied to the parent claim 17, except the recitation of a die image showing light and dark areas. The limitation that the image of the die shows light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, is well known in the art as voltage contrast defects, as recited in a large number of prior arts, e.g., by Talbot et al. as recited in the Abstract/ll.1-19 & Col.6/ll.46-48 and shown in Fig.3a-d, by Kim et al. as recited in the Abstract/ll.1-6 from bottom, and by Yamazaki et al., as recited in Col.1/ll.64-67.

It would have been obvious to adopt Talbot's or Steffan's voltage contrast defect inspection method to show light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, as taught by Kim et al. and Yamazaki et al., in order to provide a simple and speedy defect analysis so highly desirable in the semiconductor manufacturing industry.

7. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Nakasuji, Gauthier et al., Zingher and Ishihara et al.

► Claim 24 recite limitations that form a combination of claim 13 (especially regarding the step of inputting electrical signals to cause a failure in the die, e.g., as part of a durability testing and/or quality control), and claim 14 (especially regarding inputting signals in a continuous loop as part of an automation process of chip inspection, durability test and/or quality control), however, without reciting the limitation of a scanning electron microscope (SEM), the latter being recited by Talbot's and Steffan's.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's DUT board 12 to stimulate a response until a failure is induced in the die as taught by Gauthier et al., and Zingher, e.g., as part of a durability testing in a semiconductor device manufacturing process, since such testing is important for quality control, as suggested by Nakasuji.

It would have been further obvious to one of ordinary skill in the art at the time the invention was made to integrate the process by putting the data signals in a continuous loop, in order to integrate Yoshida's as modified by Gauthier et al., Zingher and Nakasuji, in a fully automated process as taught by Ishihara et al. to provide a semiconductor durability testing and/or quality control, in which failure can be examined easily, accurately and speedily, as recited by Isihara et al..

► Claim 25 recites limitations that are the same as claims 1 and 4 combined, however, without the recitation of an SEM, such combination having been previously rejected over Yoshida alone. Claim 25 is therefore obvious over Yoshida as modified

by Gauthier et al., Zingher, Nakasuji and Isihara et al., the four secondary prior arts here necessitated by the dependency on claim 24.

► Claims 26 and 27, both recite exactly the same limitations --word by word-- that are obvious over Yoshida, as recited in Col.6/ll.1-19, however, without the limitation of a scanning electron microscope (SEM) recited by Talbot's and Steffan's. Claims 26 and 27 are therefore obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al., the four secondary prior arts here necessitated by the dependency on claim 24.

► Claims 28 and 29 are also obvious over Yoshida, as recited in Col.6/ll.7-19, in which logical states are expressly recited in Col.6/ll.11-12, again, without the limitation of a scanning electron microscope (SEM) recited by Talbot's and Steffan's. Claims 26 and 27 are therefore obvious over Yoshida as modified by Gauthier et al., Zingher, Nakasuji and Ishihara et al., the four secondary prior arts here necessitated by the dependency on claim 24.

8. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Lo et al. (USPAT #6,504,393, hereinafter addressed as Lo'393).

► Claim 28 recites mostly the same limitations as claim 24, which has been previously rejected as being obvious over Yoshida, as recited above. However, Yoshida does not expressly recite an electron beam inspecting method specifically used to inspect the logical states of a plurality of circuit nodes. Lo'393 discloses an electron beam method of testing integrated circuit structures that consist a plurality of nodes, as

recited in Col.1/ll.19-36. That the nodes take on logical states is well known in the art, as disclosed, e.g., by Shiragasawa et al. in Col.10/ll.18-20. The electron beam detection of various logical states (of the nodes) is specifically recited by Yoshida in Col.6/ll.7-19.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Yoshida's electron beam inspecting method to inspect the logical states of a plurality of circuit nodes, as taught by Lo'393, since logical states of the nodes can be displayed in black and white contrast, as taught by Yoshida in Col.6/ll.2-6, thus expediting and simplifying defect identifications in a semiconductor device manufacturing process.

► Regarding claim 29, the limitations of detecting a non-positive logical state as a function of detecting an uninhibited emission of secondary electrons, and a positive logical state as a function of an inhibited emission of secondary electrons, are inherently recited by Yoshida in Col.6/ll.1-6 + ll.12-14.

Final Rejection

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is

not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Response to Applicant's Arguments

10. Applicant's arguments filed 08/23/2004 have been fully considered, but they are deemed unpersuasive. The following is Examiner's response to Applicant's arguments.

► Applicant's arguments that the previous Office Action failed to identify how the modified Yoshida reference would use an SEM in connection with the observation holes made through the backside of the die, and further, how the combined references would teach the specific limitations directed to the claimed navigating and scanning using an SEM, are deemed unpersuasive, because:

(a) It is noted that the specific features or steps upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); and

(b) Such features or steps are generally known to one of ordinary skill in the art, as implicated by Talbot et al. in Col.3/ll.13-16 & Col.6/ll.59-60 and by Steffan et al. in Col.1/ll.64-67.

► Applicant's argument that it would be impossible to replace Yoshida's EB-***tester*** with Talbot's or Steffan's equivalent device, is also deemed unpersuasive, since such an argument is obviously based on a serious misunderstanding of the examiner's rejection as well as the Yoshida's reference. As described in more details in this Office Action (see above), the examiner's suggestion is ***NOT to remove*** Yoshida's EB-tester, but to *replace* or *substitute* Yoshida's *EB (electron beam) part* of the EB-*tester* with Talbot's or Steffan's SEM, while replacing or replicating the remaining EB-tester of Yoshida's with Talbot's and Steffan's version having the same functions, but specifically designed for use with Talbot's or Steffan's SEM (instead of Yoshida's electron beam). Such a modification not only is very well possible and within skill in the art, but also expressly recited by Talbot et al. in Col.3/ll.13-16 & Col.6/ll.59-60 and by Steffan et al. in Col.1/ll.64-67.

► Applicant's argument that the combined references failed to teach an SOI structure of a wafer is quite ridiculous, because Yoshida's test object is expressly an SOI structure, as recited in the last line of the Abstract. How to combine and/or modify Yoshida's EB-testing of SOI structure with Talbot's and/or Steffan's SEM method is within skill in the art, as evidenced by the Talbot's and Steffan's references themselves, both reciting the same functions (e.g., obtaining voltage contrast data) as Yoshida's EB-testing method.

Communications

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E Souw whose telephone number is 571 272 2482. The examiner can normally be reached on Monday thru Friday, 9:00 am to 5:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 571 272 2477. The central fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications as well as for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

bes
October 29, 2004

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800